Sub Code: R2321044 **R23** **Set No. 1**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY-GURAJADA VIZINAGARAM
II B. Tech I Semester Regular/Supply Examinations, November – 2025
Digital Circuits Design
(ECE)

Time: 3 hours **Max. Marks: 70**

Question paper consists of Part A, Part B.
Part A is compulsory, Answer all questions.
In Part B, Answer any one question from each unit.
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PART-A **(20 Marks)**

1	a)	Convert the decimal number 96 to gray code	[2]
	b)	Discuss about 2 variable K-MAP	[2]
	c)	What is ripple carry adder	[2]
	d)	Which input is used to control the operation of decoder	[2]
	e)	Define Latch CO3	[2]
	f)	Draw the truth table of JK Flip Flop	[2]
	g)	What are the limitations of FSM	[2]
	h)	Define FSM	[2]
	i)	What is gate level modelling	[2]
	j)	Explain about conditional operator	[2]

PART-B **(50 Marks)**

Unit-1

2	a)	**Find all the prime** implicants **for the following Boolean functions, and determine which are essential: F (w, x, y, z) = ∑ (0, 2, 4, 5, 6, 7, 8, 10, 13, 15)**	[5]
	b)	Find the complement of the functions F1 = x'yz' + x'y'z and F2 = x(y'z' + yz).	[5]
		(OR)	
3	a)	Generate a set of prime implicants and implement it in universal logic for the function F= (1,2,3,5,6,7,8,9,12,13) using tabular method.	[5]
	b)	Demonstrate the floating point representation of real numbers	[5]

Unit-2

4	a)	Design a combinational circuit that compares two 4-bit numbers to check if they are equal. The circuit output is equal to 1 if the two numbers are equal and 0 otherwise.	[5]
	b)	Implement the given function using multiplexer. f(A,B,C,D) = ∑m (0,1,2,3,5,7,8,9,10,11,12,13,15)	[5]
		(OR)	
5	a)	Design the digital implementation of BCD adder	[5]
	b)	Demonstrate the operation of 8X3 Encoder	[5]

Unit-3

6	a)	Derive the state tables for the 4 bit ring counter	[5]
	b)	Explain the working of 3-bit bi-directional shift register with the help of diagram?	[5]
		(OR)	
7	a)	Design a 4 bit synchronous up counter	[5]
	b)	Explain the differences among a truth table, a state table, a characteristic table, and an Excitation table.	[5]

Unit-4

8	a)	Tabulate the PLA programming table for the Two Boolean functions listed below. A (x, y, z) = ∑(1, 3, 5, 6) B (x, y, z) = ∑ (0, 1, 6, 7)	[5]
	b)	What are the advantages of FPGA	[5]
		(OR)	
9	a)	Draw and explain basic structure of CPLD	[5]
	b)	Design 1010 sequence detector with overlapping	[5]

Unit-5

10	a)	Write Verilog HDL program of Full Adder	[5]
	b)	Demonstrate the working o If-Else statement	[5]
		(OR)	
11	a)	What do you mean by blocking and no blocking statements	[5]
	b)	Write Verilog HDL program of 4 bit counter	[5]